IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

AMPEX CORPORATION, Plaintiff, v. EASTMAN KODAK COMPANY, ALTEK CORPORATION and CHINON INDUSTRIES, INC., Defendants.	)	C.A. No. 04-1373-KAJ **REDACTED – PUBLIC VERSION**

<u>PROPOSED FINAL PRETRIAL ORDER</u>

VOLUME 4

MORRIS, NICHOLS, ARSHT & TUNNELL LLP
Jack B. Blumenfeld (#1014)
Julia Heaney (#3052)
1201 N. Market Street
P.O. Box 1347
Wilmington, DE 19899
(302) 658-9200
Attorneys for Plaintiff

CONNOLLY, BOVE, LODGE & HUTZ LLP
Collins J. Seitz, Jr.
1007 North Orange Street
P.O. Box 2207
Wilmington, DE 19899
(302) 658-9141
Attorneys for Defendants

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EXHIBIT 10

Defendants' Motion in Limine No. 1

DEFENDANTS' MOTION IN LIMINE TO EXCLUDE U.S. PATENT NOS. 5,016,107 AND 5,164,831 AND RELATED EVIDENCE

INTRODUCTION

Defendants move to exclude two Eastman Kodak Company patents, U.S. Patent Nos. 5,016,107 (the "'107 patent") and 5,164,831 (the "'831 patent," collectively, the "Kodak patents"), and all related evidence.[1] Ampex seeks to use these patents to misleadingly suggest that Kodak attempted to patent the same technologies covered by the asserted patent, U.S. Patent No. 4,821,121 (the "'121 patent"), long after the '121 patent was filed. The Kodak patents, however, are directed to entirely different, far more sophisticated digital camera technologies than the basic television broadcast technology described in the '121 patent. The Kodak patents are irrelevant to the issues presented by this case and Ampex's intended use of these patents would be highly prejudicial. Pursuant to Rule 403, the patents, and any related evidence, should therefore be excluded because it is more prejudicial than probative.

FACTUAL BACKGROUND

1. The Invention Claimed In The Patent-In-Suit Relates To Television Broadcast, Video Image Storage and Recall.

The '121 patent "relates to a digital electronic still store for broadcast television signals..." ('121: col. 1 ll.11-14). It discloses a system that captures an individual frame from a stream of video frames. ('121: col. 2 ll.67-69; col. 3. l.1 (video input circuit is a "source of video data from which one or more frames of a video image may be captured.")). The '121 patent does not disclose image processing of the "full size" image data input into the system - it outputs those images in the same video format it receives them. ('121: col. 3 ll.12-14; col. 4 ll.31-34). The focus of the patent is on the use of "reduced size" images, and Ampex has argued that the heart of its invention is a "fast browse" feature, that is, the ability to access and browse multiple reduced size images. (*See* D.I. 290 at 2, "The '121 patent describes a better system for rapidly generating and displaying a browse screen.").

2. The Inventions Claimed In The '107 And '831 Patents Relate To Image Capture And Processing In Digital Cameras.

The Kodak patents are directed to particular aspects of digital camera technology. Generally,

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[1] Defendants do not seek to exclude license agreements that include the '107 and '831 patents.

the Kodak patents describe and claim using a camera with a lens, sensor and circuitry to capture and digitally process image data. *The Kodak patents do not claim or even describe any "fast browse" feature.* Instead, the Kodak patents both describe and claim a digital camera with an internal image sensor called a charge-coupled device ("CCD") to capture the image information that comes through the lens in the camera when a user takes a picture. (*See, e.g.*, '107, fig.1A; col. 3 ll.31-59) (Ex. 1). The '831 patent discloses a digital camera that uses a CCD sensor to generate raw image data during still capture, and then generates and stores both high resolution and low-resolution images of the scene captured *together in one file* in permanent memory so the user can export them *together as a "single file."* REDACTED

'831: col. 8 ll.16-17 ("said combination [of different resolutions] forming a singular file structure") (Ex. 3).

The '107 patent does not even mention generating or storing reduced size images. Instead, the '107 patent discloses a digital camera that includes, *inter alia*, an input section that receives still images, which images accumulate in memory at one rate but are digitally compressed at a different rate, so that more advanced (and more time-consuming) image processing and compression techniques can be used. (*See, e.g.*, Ex. 1, col. 2 ll.45-53). Processing digital images can take time. If a user must wait for the processing of a previously captured image to be completed before a new image can be captured, there can be significant delays and a user may miss photographic opportunities. The '107 patent addresses that problem by allowing the cameras to capture images at a different and faster rate than it processes the images. (*See* Ex. 1, col. 2 ll.59-65). The '107 patent also discloses memory card and buffer diagnostics, which are nowhere found in the '121 patent.

Neither Kodak patent is asserted in this case, and neither patent is cited as prior art to the '121 patent. Attached hereto as appendix A is a chart setting forth claim 7 of the '121 patent, demonstrating the fundamental differences between claim 1 of the '831 patent and claim 1 of the '107 patent.

3. Ampex Apparently Intends To Use The Kodak Patents To Suggest That Kodak Attempted To Patent What Is Claimed In The '121 Patent After The Fact.

Throughout this litigation, Ampex and its experts have attempted to suggest that the '831 and

'107 patents indicate that Kodak tried to patent what is claimed in the '121 patent long after the application for the '121 patent was filed.

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During the ITC proceeding, Ampex also indicated it intended to offer evidence relating to the '107 and '831 patents broadly for "validity" and "infringement" purposes. (*See* Ampex's ITC Ex. list, CX-248 (offered to prove "Infringement, Claim Construction"), CX-171 (offered to prove "Claim Construction, Benefits of invention") (Ex. 5); Ampex's Motion to Compel, 6/15/05, at 8 (stating that Ampex intended to offer evidence related to the Kodak patents to prove validity of the '121 patent) (Ex. 6)). Both of these patents appear on Ampex's trial exhibit list in this action. (*See* Ampex Delaware Ex. list, PTX-737 and PTX-691) (Ex. 7).

ARGUMENT

The '107 and '831 patents are of little or no relevance to the issues in this case, and Ampex's apparent intended use of the patents would be both confusing and highly prejudicial. Pursuant to Fed. R. Evid. 403, the Kodak patents should be excluded. *See, e.g., Cordis Corp. v. Boston Scientific Corp.*, 431 F.Supp.2d 442, 459 (D. Del. 2006) (evidence relating to unasserted patent claims was properly excluded because it was more confusing than probative).

1. The '107 And '831 Patents Are Not Probative Of The Issues In This Case.

A. The '107 And '831 Patents Claim Different Technology Than The '121 Patent.

Aside from the obvious differences in the fields of digital camera and television broadcast technology that result in claims to "video" data in the '121 patent and claims to image data generated by "CCD sensors" in the '831 and '107 patents, there are additional fundamental differences that are fatal to any analogy Ampex would draw between them. With respect to the '831 patent, while the claims of that patent are directed to a technique for storing image data in different resolutions together "*as a single file*," none of the '121 patent claims require storing a full and reduced image in a single file, and this feature is nowhere even described or suggested in the '121 specification.

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Meanwhile, the claims of the '107 patent are directed to separating a digital camera's capture function from its processing function to allow for more sophisticated processing and the ability to capture additional images more quickly. The '107 patent discloses storage of only one size image data - it does not even mention thumbnails. Thus, the '107 is directed toward separate capture and processing speeds in a digital camera, while the claimed novelty of the '121 invention is to allow fast browse, or recall, of stored video images – two entirely different concepts.

B. The '107 And '831 Patents Are Not Relevant To Validity Or Infringement.

Ampex apparently intends to argue that the '121 patent is valid and not obvious because the later Kodak patents essentially claim what is claimed in the '121 patent, and thus these patents show that Kodak sought to patent Ampex's invention after the '121 patent issued. However, because the '107 and '831 patents cover different inventions from the '121 patent, *and because they are not prior art*, the Kodak patents have no bearing on the validity of the '121 patent. *See, e.g., EZ Dock, Inc. v. Schafer Sys., Inc.*, No. Civ. 98-2364 (RHK/AJB), 2003 WL 1610781 at *11 (D. Minn. 2003) (excluding Defendant's patents as not relevant to the claims of plaintiff's patent-in-suit) (Ex. 9).

The Kodak patents are not relevant to infringement for the same reason they are not relevant to validity – they disclose and claim different technologies.

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2. Ampex's Intended Use Would Be Highly Prejudicial.

Evidence pertaining to the '107 and '831 patents should be excluded under Rule 403 as both confusing and highly prejudicial. *See Glaros v. H.H. Robertson Co.*, 797 F.2d 1564, 1572-73 (Fed. Cir. 1986) (other patents properly excluded because such evidence was "likely to create side issues that would have unduly distracted the jury from the main issues."). Discussion of these two patents, which issued in the early 1990's, are not in-suit, and not prior art to the '121 patent, would merely constitute a detour from the central issues of infringement, validity and enforceability.

Specifically regarding validity, if the jury is misled into the inaccurate belief that Kodak sought to patent the claimed '121 patent technology, it could be left with the mistaken impression that Kodak believes the '121 patent has merit and value.

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Such confusion to the jury is prejudicial and it is the reason that unrelated patents are properly excluded. *Id.; see also Porous Media Corp. v. Pall Corp.*, 173 F.3d 1109, 1117-18 (8th Cir. 1999) (evidence of parties' earlier lawsuit which involved different technology in a different time period was properly excluded as prejudicial).

Because the jury easily could be confused about the import of the Kodak patents to either the '121 patent or the operation of the accused cameras, and because such confusion would infect the issues the jury is charged with deciding, the Kodak patents should be excluded. *See, Glaros*, 797 F.2d at 1572-73; *Rivera-Davila v. Asset Conservation, Inc.*, 230 F.3d 1378, 2000 WL 27891 at *5-6 (Fed. Cir. 2000) (non-infringement opinion letter written during litigation by previous trial counsel properly excluded because, although probative, such attorney argument was unfairly prejudicial) (Ex. 10); *Magnivision, Inc. v. Bonneau Co.*, 115 F.3d 956, 961 (Fed. Cir. 1997) (references to 'prosecution irregularities' should have been excluded because they were prejudicial and irrelevant to validity).

APPENDIX A

'121 patent, claim 7	**'107 patent, claim 1**	**'831 patent, claim 1**
An apparatus for storing video pixel data representing video images of a first resolution and, for each of the images at said first resolution, a corresponding video image at a second resolution, comprising: random access memory means for storing video pixel data representing one of a succession of full size images at said first resolution and a corresponding reduced size version thereof at said second resolution; bulk memory means for receiving said video pixel data from said random access memory means and for storing said succession of full size images and the corresponding reduced size versions thereof, and for outputting upon a user's command, either a selected one of the successive full size images or selected ones of the corresponding reduced size versions thereof for direct transfer to, and storage back in, said random access memory means; means responsive to said random access memory means for selectively generating one of said corresponding reduced size versions from the respective full size image in said random access memory means, and for transferring the video pixel data representing the corresponding reduced size version back to the contents of said random access memory means.	Electronic still imaging apparatus employing **digital processing** of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an **area image sensor** having a two dimensional array of photosites corresponding to picture elements of the image and **means for exposing said sensor to image light** so that analog image information if (is) generated in respective photosites, said imaging apparatus comprising: means for converting analog image information into digital image signals corresponding to the picture elements; an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images; control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an **input rate commensurate with normal operation of the camera**; **digital processing means** for operating on blocks of stored digital image signals at a **processing throughput rate different than said input rate**, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals **into a compressed stream of processed digital image signals**; means responsive to said digital processing means for downloading **the processed image signals** to said removable digital memory; and **diagnostic means** for monitoring the utilization of said image buffer whereby information is generated as to the current condition of the image buffer.	Electronic still imaging apparatus employing **digital processing** of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an **image sensor** having an array of photosites corresponding to picture elements of the still image and **means for exposing said sensor to image light** so that analog image information is generated in respective photosites, said imaging apparatus comprising: means for converting the analog image information into digital imaging signals corresponding to a predetermined picture resolution; means for subsampling said digital image signals to generate reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution; means for generating a **multi-format image file** representative of **plural resolutions of the still image** from the combination of said digital image signals and said reduced resolution image signals, said **combination forming a singular file** structure in which said reduced resolution image signals occupy a defined file area in relation to said digital image signals and are **commonly accessible therewith** for display and processing; and means for storing the image file in said digital memory.

EXHIBIT NO. 1

United States Patent [19]

Sasson et al.

[11] Patent Number: **5,016,107**

[45] Date of Patent: **May 14, 1991**

[54] ELECTRONIC STILL CAMERA UTILIZING IMAGE COMPRESSION AND DIGITAL STORAGE

[75] Inventors: Steven J. Sasson, Hilton; Robert G. Hills, Spencerport, both of N.Y.

[73] Assignee: Eastman Kodak Company, Rochester, N.Y.

[21] Appl. No.: 349,566

[22] Filed: May 9, 1989

[51] Int. Cl.^{5} H04N 5/225; H04N 5/30

[52] U.S. Cl. 358/209; 358/909; 358/906; 358/961.3

[58] Field of Search 358/479, 906, 909, 261.3, 358/427, 229, 335, 209; 360/32, 35.1

[56] References Cited

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4,489,351	12/1984	d'Alayer de Costemore d'Arc	358/213
4,541,010	9/1985	Alston	358/44
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0204626	12/1986	European Pat. Off.
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2089169	6/1988	United Kingdom

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Digital Still Video Camera Using Semiconductor Memory Card, Izawa et al., IEEE 1989, pp. 184–185.

Hashiguchi, Sumihisa, "Picture Recording and Electric Power Consumption" Shashim Kogyo, Apr. 1988, pp. 94–95.

Hashiguchi, Sumihisa, "Possibilities of the Digital Electronic Still Camera", Shashin Kogaku, Feb. 1988, pp. 110–111.

Prototype Announcement, Fijix DS–IP digital still camera, Fuji Photo Film Co., Sep. 20, 1988.

"Camera Uses E^2 PROM Film", Electronic Engineering Times, Apr. 10, 1989, p. 457.

"Ic Card Camera System–Toshiba & Fuji Photo Film" Dempa daily newspaper technical report, Mar. 20, 1989.

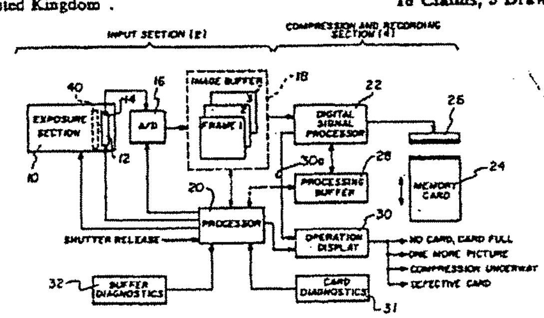
"Toshiba & Fuji Photo Film's Joint Development of Digital Still Camera System" Dempa Daily Newspaper, Mar. 24, 1989.

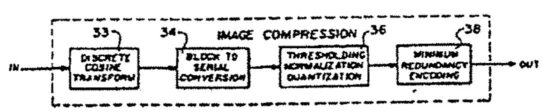
Primary Examiner—James J. Groody
Assistant Examiner—Kim Yen Vu
Attorney, Agent, or Firm—David M. Woods

[57] ABSTRACT

An electronic still camera employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. A control processor controls the exposure section and the A/D converter, delivering digital signals to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate for better image capture and optimum utilization of the camera.

18 Claims, 5 Drawing Sheets





EXHIBIT

AX203262

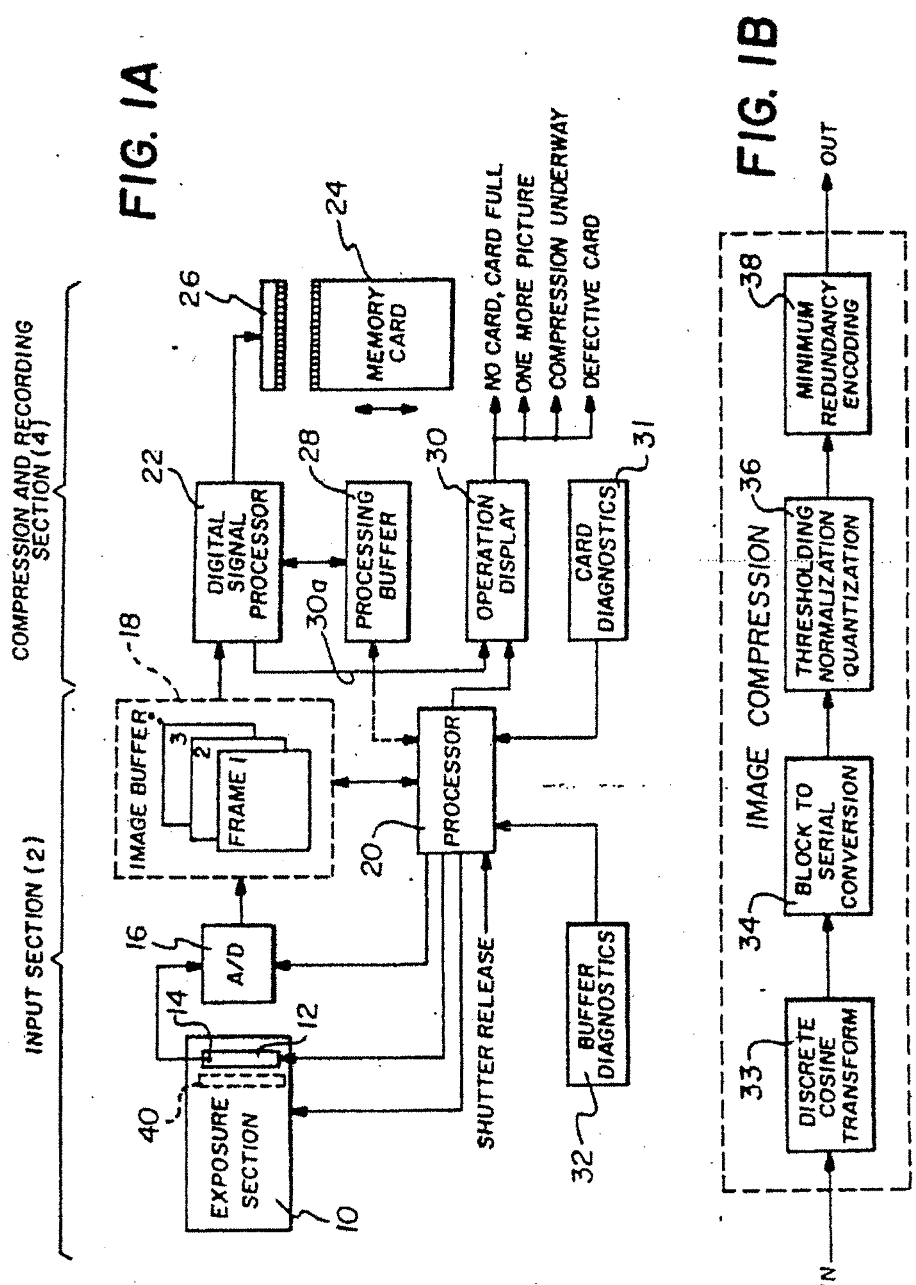

COMPRESSION AND RECORDING SECTION (4)
INPUT SECTION (2)
EXPOSURE SECTION
10
12
14
40
A/D
16
IMAGE BUFFER
FRAME 1
2
3
18
PROCESSOR
20
DIGITAL SIGNAL PROCESSOR
22
26
MEMORY CARD
24
PROCESSING BUFFER
28
30a
OPERATION DISPLAY
30
NO CARD, CARD FULL
ONE MORE PICTURE
COMPRESSION UNDERWAY
DEFECTIVE CARD
CARD DIAGNOSTICS
31
SHUTTER RELEASE
BUFFER DIAGNOSTICS
32
IMAGE COMPRESSION
IN
DISCRETE COSINE TRANSFORM
33
BLOCK TO SERIAL CONVERSION
34
THRESHOLDING NORMALIZATION QUANTIZATION
36
MINIMUM REDUNDANCY ENCODING
38
OUT

FIG. 1A

FIG. 1B

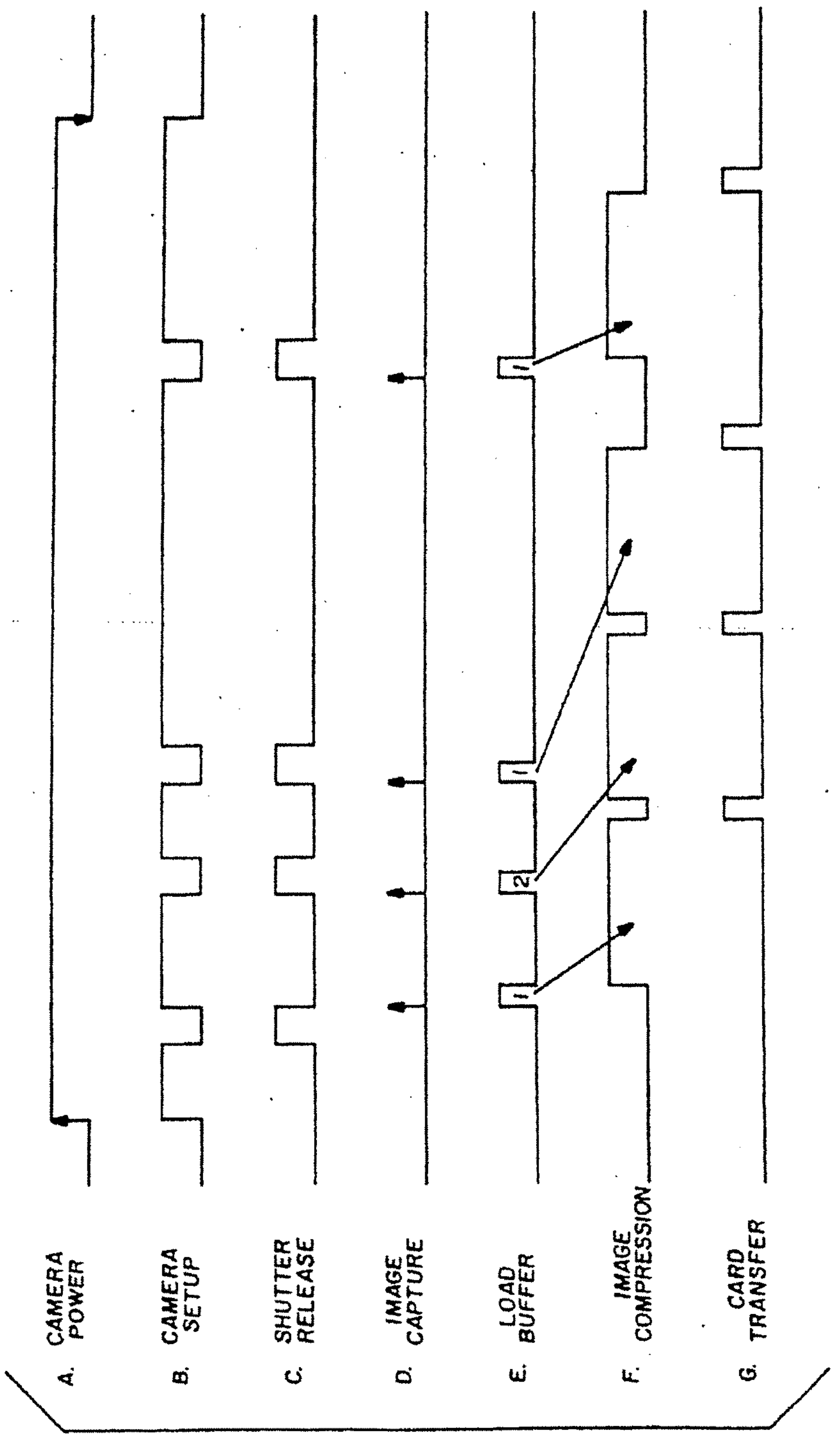

A. CAMERA POWER
B. CAMERA SETUP
C. SHUTTER RELEASE
D. IMAGE CAPTURE
E. LOAD BUFFER
F. IMAGE COMPRESSION
G. CARD TRANSFER
1
2
1
1

FIG. 2A

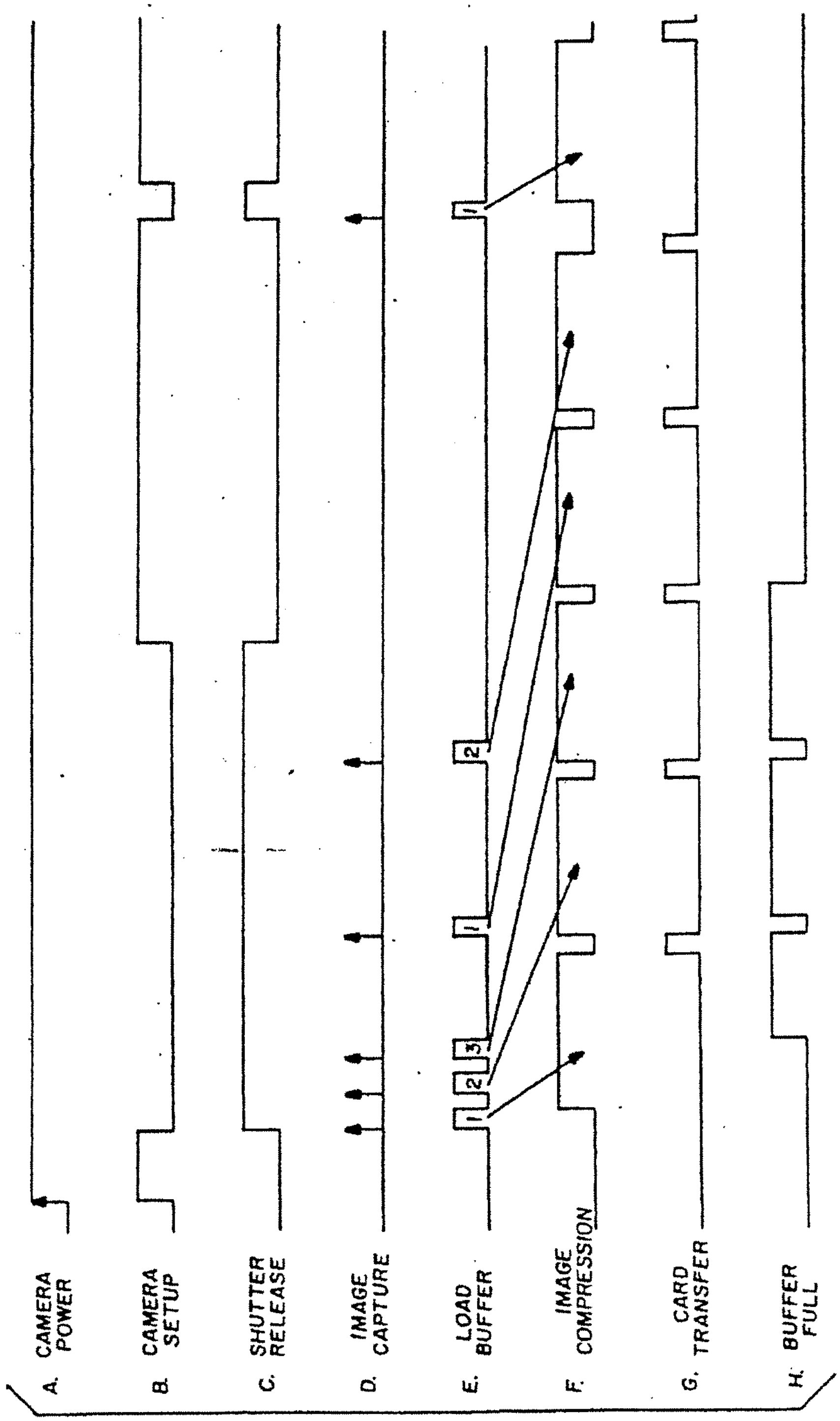


FIG. 2B

AX203265

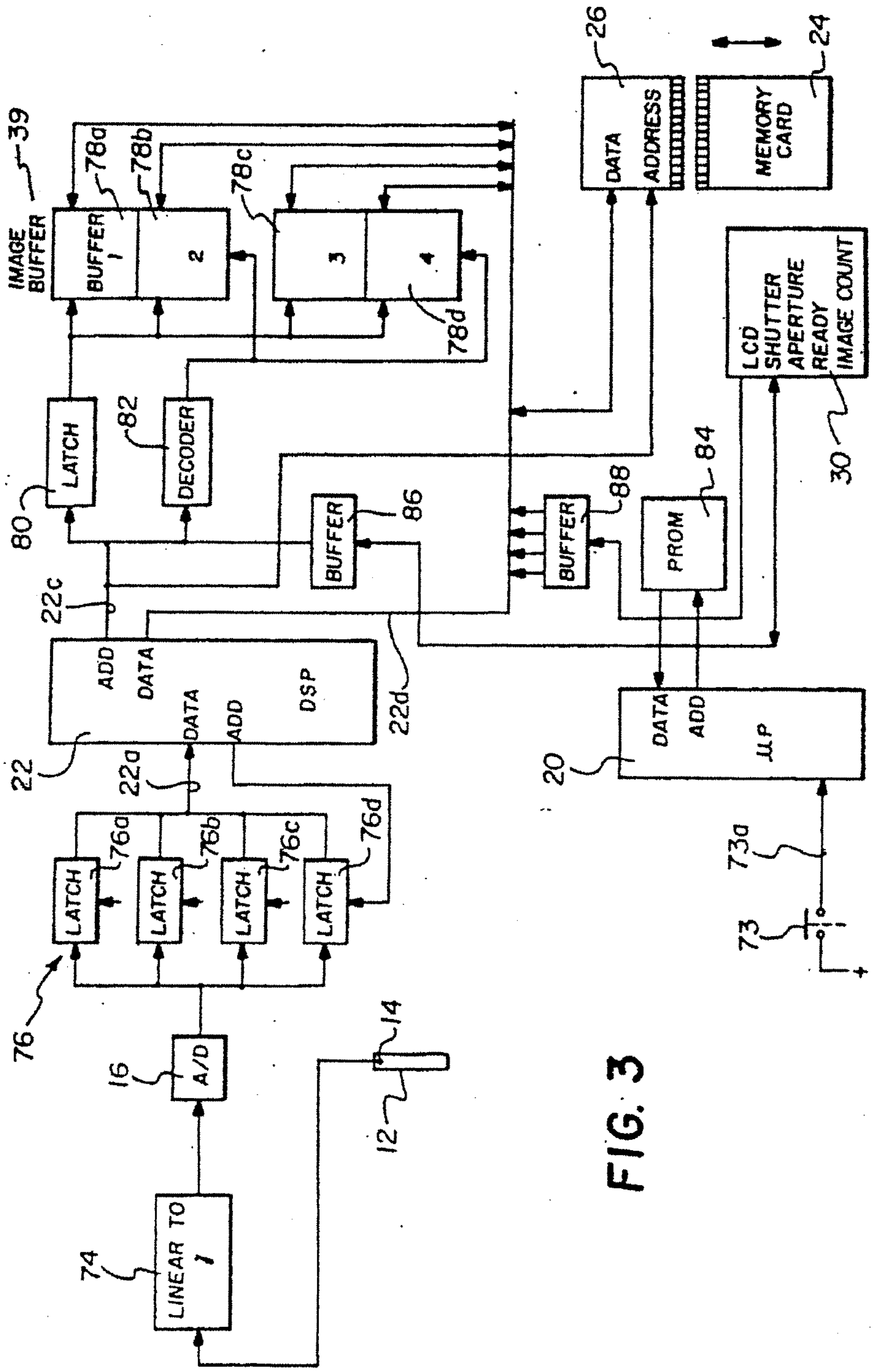
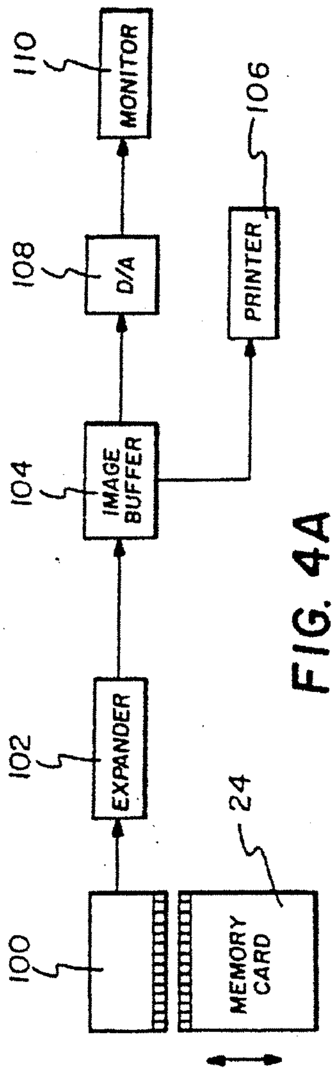


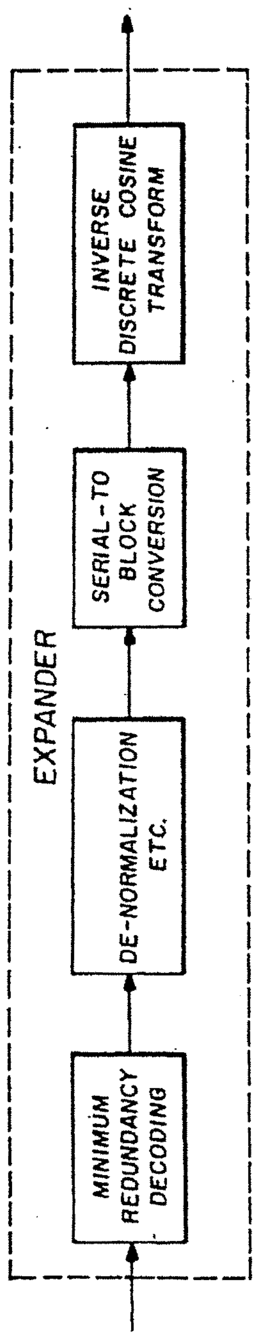
IMAGE BUFFER
39
BUFFER 1
2
3
4
78a
78b
78c
78d
DATA
ADDRESS
26
MEMORY CARD
24
LCD
SHUTTER
APERTURE
READY
IMAGE COUNT
30
LATCH
80
DECODER
82
BUFFER
86
BUFFER
88
PROM
84
22c
ADD
DATA
DSP
22
22a
22d
DATA
ADD
μP
20
73a
73
LATCH
76a
76b
76c
76d
76
A/D
16
14
12
LINEAR TO
74

FIG. 3



100
MEMORY CARD
24
102
EXPANDER
104
IMAGE BUFFER
108
D/A
110
MONITOR
PRINTER
106

FIG. 4A



EXPANDER
MINIMUM REDUNDANCY DECODING
DE-NORMALIZATION ETC.
SERIAL-TO BLOCK CONVERSION
INVERSE DISCRETE COSINE TRANSFORM

FIG. 4B

ELECTRONIC STILL CAMERA UTILIZING IMAGE COMPRESSION AND DIGITAL STORAGE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains in general to the field of electronic still imaging and, more particularly, to an electronic camera incorporating digital processing of image signals derived from an electronic image sensor and digital storage of the processed signals in a removable storage medium.

2. Description Relative to the Prior Art

An electronic still camera employing non-volatile storage of digital image signals is described in U.S. Pat. No. 4,489,351. Analog color information from three charge-coupled device (CCD) image sensors is converted into a digital bit stream and transmitted through a peripheral memory control unit to an integrated circuit memory. The memory is one unit of many, e.g., twenty-four memory units, recessed into a "cassette" that is separably attached through an electrical connector to the camera body. In order to obtain a digital image of high quality, many pixels, and thus many bits of digital information, need to be processed in a short time. In an article entitled "Possibilities of the Digital Electronic Still Camera", by Sumihisa Hashiguchi (*Shashin Kogaku*, pp. 110–111, Feb. 1988), the author proposes a multi-layer image processing integrated circuit including sensors, analog-to-digital (A/D) converters, and 8-bit buffer storage cells in respective layers. Since the output signal from an individual pixel is transferred "vertically" through an A/D converter to an included storage cell, real-time throughput is obtained without high speed operation. The stored signals can be read out slowly for digital recording, perhaps after compression, on a storage drive incorporating a small floppy disk. (Another example of a digital-based electronic still camera is shown in published UK Patent Application 2089169, in which the camera loads the digital image signals into a bubble memory cassette.)

A static random access memory (SRAM) card, in the size, and form, of a credit card, is an attractive storage alternative to the devices described in the above-related disclosures. For instance, published European Patent Application 289,944 shows a detachable SRAM module for use in a digital electronic still camera. The module is disclosed as a 32 M-bit (4 M-byte) SRAM integrated circuit card, although such storage capacities in a card are not commonly available at this time. A 512 K-byte SRAM card is presently available (Mitsubishi Electronics America, Inc. is one supplier). However, as pointed out in an article by Sumihisa Hashiguchi ("Picture Recording and Electric Power Consumption," *Shashin Kogyo*, pp. 94–95, Apr. 1988), there is a significant problem with memory volume. In the case, for example, of recording 780×490 picture elements from a CCD image sensor, with 8 bits allocated to each picture element, 382,200 bytes are required for a single monochrome video frame. This amounts to only one picture on a memory card (of 512 K-bytes). This is a considerable obstacle since still photographers are used to taking many pictures, e.g., 24 or 36 pictures, with one cassette of conventional film. Moreover, color pictures would ordinarily require three times the storage capacity of monochrome pictures.

Dynamic random access memory (DRAM) offers more storage in a reasonable volume, but power consumption quickly becomes formidable as storage capacity increases. The Hashiguchi article, consequently, calls for the development of new techniques of storage based on the compression of picture information by a factor of 10 or 100. As Hashiguchi points out, several picture compression techniques are available at present. For example, the aforementioned European Patent Application 289,944 suggests an embodiment in which a signal processor is adapted to accomplish data compression, such as the Hadamard transform, cosine transform or orthogonal transform, and coding on the video signal, which in turn is transferred to and stored interest that U.S. Pat. No. 4,131,919, which issued on Dec. 26, 1978, proposes the use of source and/or channel encoding schemes to more efficiently record digital still image signals on magnetic tape.) Adaptive differential pulse code modulation is another known compression algorithm for encoding still images.

The fundamental structure for in-camera digital processing is ordinarily based on a conventional analog camera, with digital processing techniques being applied to the functional analog blocks, such as color separation, white balance, gamma correction, and so on. This conventional transposition extends to real-time processing in that in-camera digital processing seeks, insofar as possible, to emulate real-time analog processing rates by rapidly accessing the imager, processing the resultant image signals, and writing the processed image signals to memory within normal video frame rates. (. . . albeit, that in the aforementioned *Shashin Kogaku* article of Feb. 1988, in U.S. Pat. No. 4,489,351, and in UK Patent Application 2089169, a buffer or temporary memory is provided to allow transmission of the image data to the recording device at a desired rate, which due to device or other limitations is often less than the image capture rate.) Nonetheless, as recognized by the Hashiguchi article, the available techniques neither adequately meet the requirement for real-time processing as needed by an electronic still camera nor the requirement for simply including the compression hardware with the camera.

SUMMARY OF THE INVENTION

The problem with the available techniques is their focus on real-time throughput. The present invention departs from this focus by distinguishing the input function of the camera from the processing function so that, on the one hand, image signals from a plurality of still images accumulate at a rate commensurate with normal operation of the camera while, on the other hand, the accumulated image signals are digitally processed at a throughput rate different than the accumulating rate. The prior techniques tend, by nature of their focus upon speed, not only to direct compression choices to those capable of handling a data stream at an extremely fast rate, such as differential pulse code modulation (DPCM), but also tend to focus processing upon one image at a time. By providing a multi-image input buffer and separating digital processing from input requirements, the digital processor not only has more time to operate on blocks of image signals, in particular transform encoding the blocks of signals, but also obtains such processing advantages without disturbing the "stacking up" of images in the input buffer. The invention further utilizes a removable digital storage means, such as a SRAM memory card, to store the compressed image signals. With 10:1 compression, for example, the

byte requirement for a picture can be reduced by a factor of ten and many more images can be stored in the memory card.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, in which:

FIG. 1A is a block diagram of an electronic still camera employing digital processing according to the invention;

FIG. 1B is a block diagram of an exemplary form of image compression used in connection with the invention;

FIG. 2A is a functional sequence diagram showing multi-image input buffering;

FIG. 2B is a further functional sequence diagram showing full utilization of the input buffer and concomitant delay;

FIG. 3 is a block diagram showing details of a specific processing architecture for the electronic still camera;

FIG. 4A is a block diagram of an electronic still player for use in reproducing pictures taken with the camera of FIG. 1A; and

FIG. 4B is a block diagram of an exemplary form of image expansion used in connection with the player of FIG. 4A.

DETAILED DESCRIPTION OF THE INVENTION

Because electronic still cameras employing charge-coupled device (CCD) sensors are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIGS. 1A and 1B, an electronic still camera is divided generally into an input section 2 and a compression and recording section 4. The input section 2 includes an exposure section 10 for directing image light from a subject (not shown) toward an image sensor 12. Although not shown, the exposure section 10 includes conventional optics for directing the image light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The sensor 12, which includes a two-dimensional array of photosites corresponding to picture elements of the image, is a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. The sensor 12 is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode 14, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter 16, which generates a digital image signal from the analog input signal for each picture element.

The digital signals are applied to an image buffer 18, which is a random access memory (RAM) with storage capacity for a plurality of still images. The arrangement for allocating memory space in the image buffer 18 to individual frames may vary; for this description, however, the frames will be allocated to specific, identifiable memory spaces such that a new frame can be directly written over an old frame without affecting the other frames in the buffer 18. This, as will be shown, becomes convenient in unloading the buffer 18 and freeing memory space for a new frame as soon as the older ones are processed.

A control processor 20 generally controls the input section 2 of the camera by initiating and controlling exposure (by operation of the diaphragm and shutter (not shown) in the exposure section 10), by generating the horizontal and vertical clocks needed for driving the sensor 12 and for clocking image information therefrom, and by enabling the A/D converter 16 in conjunction with the image buffer 18 for each signal segment relating to a picture element. (The control processor 20 would ordinarily include a microprocessor coupled with a system timing circuit.) Once a certain number of digital image signals have been accumulated in the image buffer 18, the stored signals are applied to a digital signal processor 22, which controls the throughput processing rate for the compression and recording section 4 of the camera. The processor 22 applies a compression algorithm to the digital image signals, and sends the compressed signals to a removable memory card 24 via a connector 26. A representative memory card is a 512 K-byte static random access memory (SRAM) available from Mitsubishi Corp.

Since the compression and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer 28. (The processing buffer 28 may also be configured as part of the memory space of the image buffer 18.) The number of image signals needed in the image buffer 18 before digital processing can begin depends on the type of processing, that is, for a block transformation to begin, a block of signals including at least a portion of the image signals comprising a video frame must be available. Consequently, in most circumstances, the compression may commence as soon as the requisite block, e.g., of 16×16 picture elements, is present in the buffer 18.

The input section 2 operates at a rate commensurate with normal operation of the camera while compression, which consumes more time, can be relatively divorced from the input rate. The exposure section 10 exposes the sensor 12 to image light for a time period dependent upon exposure requirements, for example, a time period between 1/1000 second and several seconds. The image charge is then swept from the photosites in the sensor 12, converted to a digital format, and written into the image buffer 18 during a standard rate, which may, for example, correspond to a standard video field or frame rate. The repetition rate of the driving signals provided by the control processor 20 to the sensor 12, the A/D converter 16 and the buffer 18 are accordingly generated to achieve such a transfer. The processing throughput rate of the compression and recording section 4 is determined by the character of an image, i.e., the amount of detail versus redundant information, and the speed of the digital signal processor 22, and may take up to several seconds for an especially complex image.

One desirable consequence of this architecture is that the processing algorithm employed in the compression and recording section may be selected for quality treatment of the image rather than for throughput speed. This, of course, can put a delay between consecutive pictures which may affect the user, depending on the time between photographic events. This is a problem since it is well known and understood in the field of still video recording that a digital still camera should pro-

vide a continuous shooting capability for a successive sequence of images. For this reason, the image buffer 18 shown in FIG. 1 provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. The size of the buffer is established to hold enough consecutive images to cover most picture-taking situations. FIGS. 2A and 2B show the typical functional sequence for a camera having buffer area for three separate images. As each image is captured (line D), the next available buffer area is loaded (line E) and image compression begins (line F). FIG. 2A illustrates a typical situation in which the shutter release (line C) is actuated at spaced times insufficient to load all three buffer areas. In FIG. 2B, the shutter release is continuously held down (line C) and a burst of exposures ensue. The three buffer areas are quickly loaded (line E) and, responsive to a buffer full signal (line H), the control processor 20 interrupts the exposure section 10. No further image is then captured until a buffer is freed. For example, in lines E and F, after the first image is compressed and transferred to the card 24, the first buffer area is freed up and a fourth exposure is made.

An operation display panel 30 is connected to the control processor 20 for displaying information useful in operation of the camera. Such information might include typical photographic data, such as shutter speed, aperture, exposure bias, color balance (auto, tungsten, fluorescent, daylight), field/frame, low battery, low light, exposure modes (aperture preferred, shutter preferred), and so on. Moreover, other information unique to this type of camera is displayed. For instance, the memory card 24 would ordinarily include a directory signifying the beginning and ending of each stored image. This would show on the display 30 as either (or both) the number of images stored or the number of image spaces remaining, or estimated to be remaining.

The control processor 20 also accesses a card diagnostics memory 31 for generating important information about the condition of the memory card 24. Specifically, the connector 26 is queried for the presence of a card 24 and, if no card is connected, a "no card" display is produced on the operation display 30. Likewise, if a card is present but it is full of images, a "card full" display is produced. The card diagnostics memory 31 also provides a verification routine to check the card 24 for faults or defects. For instance, a set of code patterns (such as 010101 . . . and 101010 . . .) can be written into and read from the card to verify memory locations. This is especially important since compressed data is stored on the card 24 and even one defective memory location can produce an extensive visual artifact in the expanded picture. If a card 24 fails the verification test, a "defective card" display is produced on the operation display 30.

Buffer diagnostics are maintained in a memory 32 for producing certain information about the condition of the image buffer 18. Its principal purpose is to monitor the utilization of buffer space and produce, as shown in line H of FIG. 2B, a "buffer full" signal when no more buffer space is available. A corresponding display is produced on the display 30, which is important to the user as no further image can be captured until a buffer area is freed up. The digital signal processor 22 further provides a signal indicative of the compression operation on a line 30a to the operation display 30, that is, a signal indicating that compression is underway. A corresponding display, "compression underway", is activated by the display 30.

The digital signal processor 22 compresses each still video image stored in the image buffer 18 according to a known image compression algorithm shown in FIG. 1B. The compression algorithm begins with a discrete cosine transformation (block 33) of each successive block of the image data to generate a corresponding block of cosine transform coefficients. It is well-known that compression techniques are greatly enhanced when applied to image data which has been previously transformed in accordance with a discrete cosine transform algorithm. The cosine transform coefficients are then rearranged in serial order by a block-to-serial conversion step (block 34) described and illustrated in U.S. Pat. No. 4,772,956, "Dual Block Still Video Compander Processor," issued Sept. 20, 1988 to Roche et al., and which is assigned to the assignee of the present invention and incorporated by reference into the present patent application. The block-to-serial conversion step consists of arranging the discrete cosine transform coefficients in order of increasing spatial frequency, which corresponds to a zig-zag pattern illustrated in the Roche et al patent. The resulting serial string of transform coefficients is then subjected to thresholding, normalization, and quantization (block 36) and minimum redundancy encoding (block 38).

Thresholding discards data words of magnitudes less than a threshold number. Normalization entails dividing each data word by a divisor to yield a quotient. Quantization discards the fractional bits in the quotient. Minimum redundancy encoding is a technique well-known in the prior art and employs two complimentary steps, namely amplitude encoding and run length encoding. Amplitude encoding (or "Huffman Encoding") assigns to each of a finite set of possible amplitudes an encoded bit pattern designed to require the smallest number of bits for non-redundant representation. Run length encoding represents any consecutive run of zeros in the data as the smallest non-redundant bit pattern required to count the number of zeros in the run. The set of bit patterns representing each of the possible word amplitudes and the set of bit patterns representing each of the possible zero run lengths may be selected in accordance with the well-known principles and stored in look-up tables for use during the compression process. This compression technique greatly reduces the number of bits required to represent a frame of still video information, without reduction in image quality, thereby greatly reducing the amount of storage that must be allocated to each still frame in the SRAM card 24.

The uncompressed still video data stored in the image buffer 18 is organized in the manner of a television picture, that is, in vertical columns and horizontal rows of video data bytes (representing the corresponding picture elements) divisible into square blocks of bytes, each block comprising, e.g., 16 columns and 16 rows of bytes. The control processor 20 fetches a block of data each time the digital signal processor 22 is about to execute the compression algorithm. The compression process eliminates many bits contained in each block of video data, so that the compressed video data does not emerge from the processor 22 as a standard-length stream of bits, but as a variable number of bits dependent upon the complexity of the picture and the rules used for truncating bits. The memory space, therefore, allocated for each image in the SRAM card 24 can vary from image to image. The processor 22, consequently,

allocates memory space in the SRAM card 24 after each compression sequence for an image is completed so that the images may be "packed" into the card as a continuum of compressed image data. This means the storage capacity, in terms of actual images, of the SRAM card is unknown in the beginning, and then gradually is specified as pictures are taken and the card is "filled". The control processor 20 monitors the numbers of images, furnishing a running total to the operation display panel 30, and further triggers a special "one more picture" display when the remaining memory space is sufficient for a predetermined number of, say one more, pictures. Alternatively, a fixed "maximum" space can be allocated in the SRAM card 24 for each image; in this case, fewer images can be stored although the total capacity is always known.

What has been described to this point applies equally to monochrome or color pictures, except that color pictures require additional processing. For instance, if a multi-spectral color filter array (shown in broken line 40 in FIG. 1A) overlies the image sensor 12, the various colors are sorted out and processed differently for each color. This would be accomplished by an additional routine in the digital signal processor 22. Such color filter array processing would precede the discrete cosine transform block 33 (FIG. 1B) so that image compression can be done separately on each color and three compressed frames would be stored in the memory card 24 for each image.

FIG. 3 illustrates details of a specific processing architecture in which an image buffer 39 combines the function of the image buffer 18 and the processing buffer 28 shown in FIG. 1A. The analog signals from the output diode 14 of the image sensor 12 are gamma-corrected in a conventional linear-to-gamma correction circuit 74 and applied to the A/D converter 16. The output of the A/D converter 16 is connected to an 8 bit-to-32 bit latching array 76 comprising latches 76*a*, 76*b*, 76*c*, and 76*d*. In practice, the latching array 76 performs a double buffering operation to save time, that is, the latched bytes are unloaded in pairs to the processor 22 on a 32 bit-wide input data bus 22*a*, as follows. After latches 76*a* and 76*b* are loaded with the first two bytes provided by the A/D converter 16, the latched bytes are applied in parallel to the data bus 22*a*. In the meantime other two latches 76*c* and 76*d* are being loaded with the next two bytes. When the latches 76*c* and 76*d* are full, the latched bytes are applied in parallel to the input data bus 22*a* while the other latches 76*a* and 76*b* are being loaded with new bytes.

In this architecture, therefore, the digital signal processor 22 has the initial function, prior to compression, of transferring the paired input bytes to the image buffer 39, which includes random access memories (RAMs) 78*a*, 78*b*, 78*c*, and 78*d*. In terms of allocating bytes to storage, RAM 78*a* receives data from the latch 76*a*, RAM 78*b* from latch 76*b*, and so on. The digital signal processor 22 produces address words on an address bus 22*c* connected to the RAMs 78*a*–78*d*. The address word is held in an address latch 80 while a portion of the address word is decoded in a decoder 82 for activating the appropriate chip enable ports of the image buffer RAMs 78*a*–78*d*. As shown in FIG. 3, the buffer 39 is enabled in pairs of RAMs 78*a*–78*d* to correspond to the paired bytes being transferred from the latches 76*a*–76*d*.

The embodiment of FIG. 3 includes no resident non-volatile memory for the digital processor 22. Consequently, the operating program code for the camera is stored in a programmable read only memory (PROM) 84 connected to the address and data buses of the control processor 20. These bus lines are also connected, through respective buffers 86 and 88, to the output address bus 22*c* and the output data bus 22*d* of the digital processor 22. The control processor 20 downloads portions of the operating program from the PROM 84 to the image buffer 39 as required for operation of the digital processor 22. For instance, when a shutter release 73 is depressed and a line 73*a* is activated, the control processor 20 downloads the data acquisition code over the data bus 22*d* to a specified location in the image buffer 39. The appropriate address words are then applied to the address bus 22*c* by the control processor 20 and the operating code is written into volatile memory in the digital processor 22. The processor 22 is then ready to latch incoming image bytes into the latch array 76 and transfer paired bytes to the image buffer 39.

When all the image bytes of a still picture are in the image buffer 39, the control processor 20 downloads the operating code for the discrete cosine transform from the PROM 84 to a specified unused memory space in the image buffer 39. The DCT code is written into the volatile memory of the processor 22 and the discrete cosine transformation is performed on blocks of image bytes in the image buffer 39. After each block is transformed, the transform coefficients are written back into the image buffer 39. The control processor 20 next downloads the operating code for the block to serial conversion in like manner, the conversion is performed, and the serial string is written back into the buffer. Then the code for thresholding, normalization and quantization is downloaded in similar fashion, the processing done and processed data stored, and the code for minimum redundancy encoding is downloaded and the amplitude and run length encoding is done. With the image data now in its finally compressed form, and instead of writing the compressed data back into the buffer 39 one more time, the compressed data is directly written into the memory card 24. The above-related technique for storing the operating code in the PROM 84 and downloading sections thereof as needed conserves on the need for fast, and therefore expensive, non-volatile memory dedicated to the processor 22.

A simplified block diagram is shown in FIG. 4*a* of a still video player for reproducing a picture or for making a hard copy print from the digital image signals stored in compressed format in the memory card 24. With the card 24 inserted into a connector 100, the digital signals are accessed and processed in an expander 102. An expansion algorithm, which is basically the inverse of the compression algorithm of FIG. 1B, is shown in FIG. 4B and implemented by the expander 102. The digital image data is expanded block-by-block and stored in an image buffer 104 as a decompressed image. A conventional thermal printer 106 is connected to the buffer 104 for making a hard copy thermal print from the decompressed image. In addition, the decompressed image signals are converted to analog form by a digital-to-analog (D/A) converter 108 and displayed on a conventional CRT monitor 110.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

What is claimed is:

1. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information if generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory; and

diagnostic means for monitoring the utilization of said image buffer whereby information is generated as to the current condition of the image buffer.

2. The apparatus claimed in claim 1 in which said diagnostic means includes means for monitoring the remaining storage capacity of said image buffer.

3. The apparatus as claimed in claim 2 in which said diagnostic means includes means for providing a buffer full signal when said buffer is fully loaded.

4. The apparatus as claimed in claim 3 wherein said control processor means includes means responsive to said buffer full signal for interrupting said exposing means and preventing further exposure of said image sensor.

5. The apparatus as claimed in claim 3 further including a visual indicator and wherein said control processor means activates said visual indicator according to the state of said buffer full signal.

6. The apparatus as claimed in claim 1 in which said digital processing means further includes a processing buffer, said digital processing means operating on blocks of digital image signals before said image buffer is fully loaded and storing intermediate products of said processing in said processing buffer so that memory space is freed in said image buffer for further storage of new still images.

7. The apparatus as claimed in claim 1 which said digital processing means generates in operating signal indicating when the compression algorithm is operating.

8. The apparatus as claimed in claim 7 further including a visual indicator and wherein said control processor means activates said visual indicator according to the state of said operating signal.

9. The apparatus as claimed in claim 1 in which said digital processing means compresses the digital image signal in a plurality of stages, one stage including the performance of a discrete cosine transform on the blocks of image signals and another stage including minimum redundancy encoding of the transformed image signals.

10. An electronic still camera employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said camera including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image signals are obtained from the respective photosites, said camera comprising:

an A/D converter for converting the analog image signals into digital image signals;

a digital processor for processing the digital image signals through a compression algorithm and for generating a stream of compressed signals having a variable bit length dependent upon the character of the image, said processor allocating a variable-length memory space in said removable digital memory for each image;

means for downloading the compressed signals to the allocated image space such that consecutive memory spaces may differ in length depending on the character of each image; and

means for generating a warning signal when the remaining unused memory space in said removable digital memory corresponds to a predetermined amount of memory space generally suitable for at least one more still image.

11. The camera as claimed in claim 10 further including a visual indicator and means for activating said visual indicator according to the state of said warning signal.

12. An electronic still camera employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said camera including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image signals are obtained from the respective photosites, said camera comprising:

an A/D converter for converting the analog image signals into digital image signals;

a random access image buffer having memory space sufficient for a plurality of still images;

control means responsive to repeated actuation of said exposing means for entering the digital image signals corresponding to a sequence of still images into said image buffer at a rate commensurate with normal operation of the camera, said control means intermittently disabling and reenabling said exposing means according to the memory space remaining in said random access image buffer;

a digital processor for compressing the digital image signals, said processor connected to said buffer for operating on stored digital signals from the first stored image irregardless of the entering of digital

signals corresponding to subsequent still images into said buffer; and

means responsive to said digital processor for downloading the compressed image signals to said removable digital memory.

13. The camera as claimed in claim 12 in which said digital processor operates a compression algorithm on blocks of stored digital signals corresponding to blocks of picture elements, said block compression operating irregardless of the entering of digital signals corresponding to further blocks of the same image.

14. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory; and

diagnostic means for checking the removable digital memory for faults or defects.

15. The apparatus as claimed in claim 14 in which said diagnostic means includes means for providing a defective card signal whenever the removable digital memory fails the check provided by said diagnostic means.

16. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer for storing one or more blocks of digital image signals corresponding to portions of a still image;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer;

digital processing means for operating on each block of stored digital image signals, said digital processing means including means for transforming each block of digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals;

diagnostic means for checking the removable digital memory for faults or defects and for providing an indication thereof; and

means responsive to said digital processing means and to said indication from said diagnostic means for downloading the processed image signals to said removable digital memory.

17. The apparatus as claimed in claim 16 in which said diagnostic means includes means for providing a defective card warning signal whenever the removable digital memory fails the check provided by said diagnostic means.

18. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said area image sensor including a color filter array having a multi-colored pattern oriented to said photosites and including one color representative of luminance, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to the picture elements;

an image buffer with storage capacity for storing digital image signals corresponding to a plurality of still images;

control processor means responsive to user instructions for initiating operation of said exposing means, for clocking the image information from said sensor, and for controlling said converting means to deliver said digital signals to said image buffer, said control processor means loading digital image signals corresponding to said plurality of still images into said image buffer at an input rate commensurate with normal operation of the camera;

digital processing means for operating on blocks of stored digital image signals at a processing throughput rate different than said input rate, said digital processing means including means for transforming blocks of digital signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a compressed stream of processed digital image signals, said digital processing means interpolating at least the luminance component over the block area and transforming each block of digital signals including the interpolated signals; and

means responsive to said digital processing means for downloading the processed image signals to said removable digital memory.

* * * * *

EXHIBIT NO. 2

EXHIBIT NO. 2

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EXHIBIT NO. 3

US005164831A

United States Patent [19]

Kuchta et al.

[11] Patent Number: 5,164,831

[45] Date of Patent: Nov. 17, 1992

[54] ELECTRONIC STILL CAMERA PROVIDING MULTI-FORMAT STORAGE OF FULL AND REDUCED RESOLUTION IMAGES

[75] Inventors: Daniel W. Kuchta, Brockport; Peter J. Sucy, Hamlin, both of N.Y.

[73] Assignee: Eastman Kodak Company, Rochester, N.Y.

[21] Appl. No.: 494,205

[22] Filed: Mar. 15, 1990

[51] Int. Cl.⁵ H04N 5/30

[52] U.S. Cl. 358/209; 358/102; 358/909; 358/432; 360/35.1

[58] Field of Search 358/432, 909, 906, 403, 358/433, 445, 447, 448, 452, 458, 133, 459, 209, 471, 102; 360/33.1, 35.1

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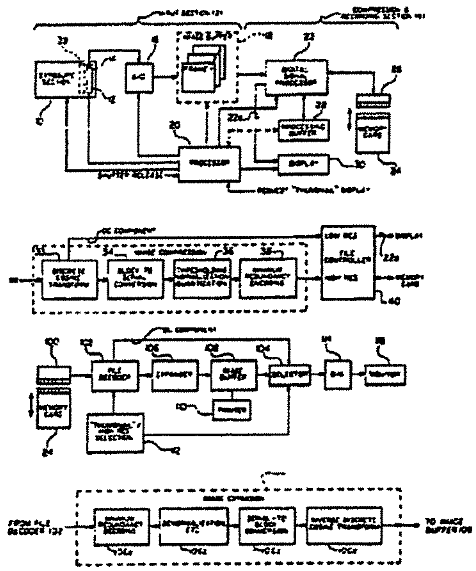
Primary Examiner—James J. Groody
Assistant Examiner—Jeffrey S. Murrell
Attorney, Agent, or Firm—David M. Woods

[57] ABSTRACT

An electronic still camera employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. A control processor controls the exposure section and the A/D converter, delivering digital signals to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate for better image capture and optimum utilization of the camera.

15 Claims, 3 Drawing Sheets



EXHIBIT
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eb 5-25-05

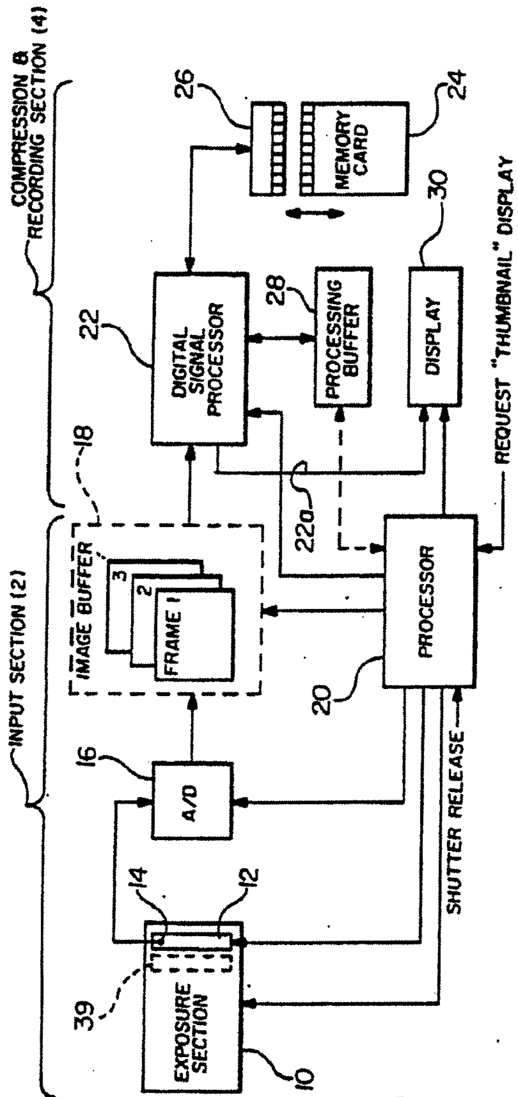
COMPRESSION & RECORDING SECTION (4)
INPUT SECTION (2)
EXPOSURE SECTION
A/D
IMAGE BUFFER
FRAME 1
2
3
DIGITAL SIGNAL PROCESSOR
PROCESSING BUFFER
MEMORY CARD
DISPLAY
PROCESSOR
SHUTTER RELEASE
REQUEST "THUMBNAIL" DISPLAY
10
12
14
16
18
20
22
22a
24
26
28
30
39

FIG. 1A

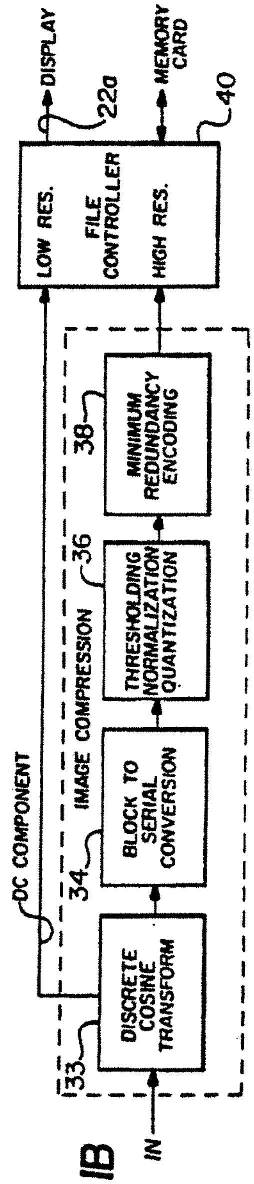
IN
DISCRETE COSINE TRANSFORM
BLOCK TO SERIAL CONVERSION
THRESHOLDING NORMALIZATION QUANTIZATION
MINIMUM REDUNDANCY ENCODING
IMAGE COMPRESSION
DC COMPONENT
LOW RES.
FILE CONTROLLER
HIGH RES.
DISPLAY
MEMORY CARD
22a
33
34
36
38
40

FIG. 1B

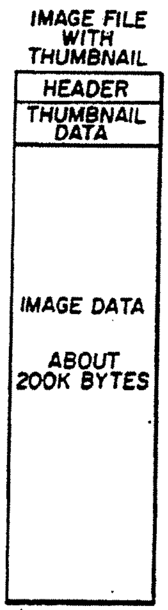

FIG. 2A

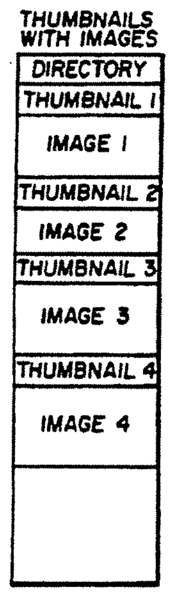

FIG. 2B

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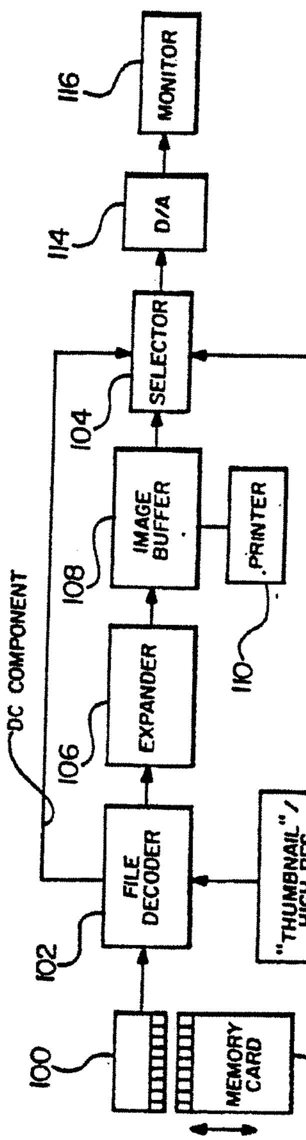
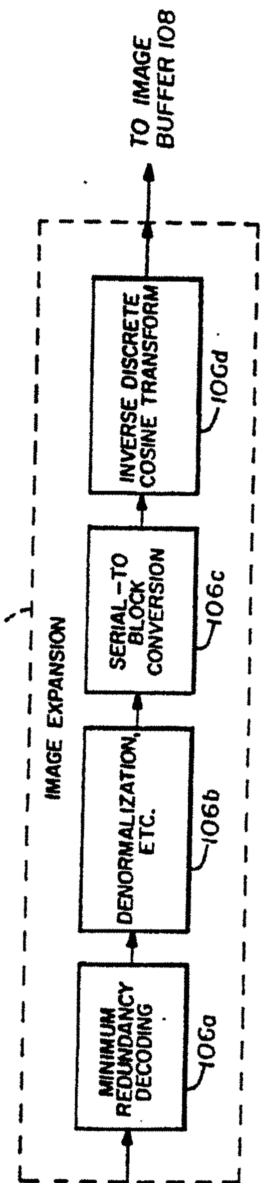


100
MEMORY CARD
24
102
FILE DECODER
DC COMPONENT
106
EXPANDER
108
IMAGE BUFFER
PRINTER
110
104
SELECTOR
114
D/A
116
MONITOR
"THUMBNAIL"/ HIGH RES. SELECTION
112

FIG. 3A



FROM FILE DECODER 102
106
IMAGE EXPANSION
MINIMUM REDUNDANCY DECODING
106a
DENORMALIZATION, ETC.
106b
SERIAL-TO BLOCK CONVERSION
106c
INVERSE DISCRETE COSINE TRANSFORM
106d
TO IMAGE BUFFER 108

FIG. 3B

ELECTRONIC STILL CAMERA PROVIDING MULTI-FORMAT STORAGE OF FULL AND REDUCED RESOLUTION IMAGES

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains in general to the field of electronic still imaging and, more particularly, to apparatus incorporating digital processing of image signals derived from an electronic image sensor and digital storage of the processed signals.

2. Description Relative to the Prior Art

An electronic still camera employing non-volatile storage of digital image signals is described in copending U.S. patent application Ser. No. 349,566, filed May 9, 1989 now U.S. Pat. No. 5,016,107 dated May 1, 1991, and assigned to the same assignee as the present invention. The electronic still camera disclosed therein employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a removable static random access memory card. An image sensor is exposed to image light and the resultant analog image information is converted to digital image signals. The digital signals are delivered to a multi-image buffer at a rate commensurate with normal operation of the camera. A digital processor operates on the stored digital signals, transforming blocks of the digital signals and encoding the signals into a compressed stream of processed image signals, which are downloaded to the memory card. The digital processor operates at a throughput rate different than the input rate, thereby allowing more efficient image capture and optimum utilization of the camera.

Despite efficient operation of such a camera and the use of compression to reduce the amount of data, high quality digital image files written in the memory card are nonetheless quite large and take significant amounts of time to process due to image size, image resolution, and the nature of the compression process. For example, a 1,280 by 1,024 pixel, 24-bit per pixel image might compress over many seconds to 100 to 300 Kilobytes of storage area. It is often desirable to quickly review the images on the memory card before deciding to transmit, to make a copy, or to retake a picture. The physical time for decompression and display of a high resolution image can be so slow as to interfere with the review process.

The matter of electronic preview has been taken up in a number of prior art disclosures. For instance, in U.S. Pat. No. 4,827,347 an electronic still camera includes a Plurality (twelve) of small displays connected to a like plurality of display/framestores so that pictures can be previewed as a group and then individually retained or discarded. The aforementioned processing time problem, however, is not addressed. In U.S. Pat. No. 4,763,208, an electronic still camera cooperates with playback apparatus that subsamples images recorded on a disk and simultaneously displays the subsampled images as a group on a monitor. While with this construction the contents of the disk can be searched within a shorter time, the subsampled images are unavailable for subsequent review. Research Disclosure item 28618 (p. 71 of the February, 1988 issue) describes a concept for storing video signals from electronically scanned negatives on individual tracks of a video disk while simultaneously storing miniature versions of these pictures in a mosaic frame store. After all the images are recorded on their individual tracks, and the mosaic frame store is accordingly filled, the mosaic-like content of the frame store is itself recorded as a full NTSC frame on a separate track. A similar concept is applied to an all-video picture processing system in U.S. Pat. No. 4,802,019 for rearranging, replacing, or inserting video programs in a sequence of such programs. Each program is characterized by a single frame that is reduced or "squeezed" to one sixteenth its original size and included in a mosaic of like pictures on an index screen. Rearrangement, etc. of the video programs is then made by reference to the index screen. In the latter two systems, the miniaturized pictures are stored together as a video frame. This is of little aid in an all-electronic system in which the pictures are, for example, separately transmitted to a remote location, separately edited, or otherwise used in a way in which continued, rapid review of a particular recorded picture is desirable.

SUMMARY OF THE INVENTION

The invention is based on the addition of a reduced resolution image to the digital file format for an individual high resolution image. Particularly if the reduced resolution, or "thumbnail", image is created as a part of the image acquisition process, or in close timing thereto, it is convenient to provide multi-format storage of the "thumbnail" image in a reserved area associated with each image file. The "thumbnail" image then follows the high resolution image wherever the image file travels. Since the "thumbnail" image is easily and quickly accessed, reviewing and display is extremely fast.

In accordance with the invention, electronic still imaging apparatus employs digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory. The imaging apparatus also includes an image sensor having an array of photosites corresponding to picture elements of the image and means for exposing said sensor to image light so that analog image information is generated in respective photosites. The analog image information is converted into digital image signals and, further, reduced resolution signals are generated from the digital image signals. A multi-format image file is formed by combining the (full resolution) digital image signals and the reduced resolution signals. The image file is then stored in the digital memory, where the reduced resolution signals may be quickly accessed for rapid display.

In accordance with a further embodiment of the invention, electronic still image processing apparatus includes an image buffer with storage capacity for storing digital image signals corresponding to a still image. A digital processor transforms blocks of the stored digital image signals into corresponding sets of transform coefficient signals and encodes the coefficient signals into a compressed stream of processed image signals. In addition, the digital processor generates reduced resolution image signals from the stored digital image signals and downloads both the processed (high resolution) image signals and the reduced resolution image signals to a digital memory. In a preferred implementation, the reduced resolution signals are based on the average or dc component coefficient signals generated during the transformation.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in relation to the drawings, in which:

FIG. 1A is a block diagram of an electronic still camera employing digital processing and multi-format storage according to the invention;

FIG. 1B is a block diagram of an exemplary form of image compression used in connection with the invention;

FIG. 2A is a diagram of a preferred file format for a single full resolution image and its associated "thumbnail" image;

FIG. 2B is a diagram of a preferred file format for several full resolution images and their associated "thumbnail" images;

FIG. 3A is a block diagram of an electronic still player for use in reproducing pictures taken with the camera of FIG. 1A; and

FIG. 3B is a block diagram of an exemplary form of image expansion used in connection with the player of FIG. 3A.

DETAILED DESCRIPTION OF THE INVENTION

Because electronic still cameras employing charge-coupled device (CCD) sensors are well known, the present description will be directed in particular to elements forming part of, or cooperating more directly with, apparatus in accordance with the present invention. Elements not specifically shown or described herein may be selected from those known in the art.

Referring initially to FIGS. 1A and 1B, an electronic still camera is divided generally into an input section 2 and a compression and recording section 4. The input section 2 includes an exposure section 10 for directing image light from a subject (not shown) toward an image sensor 12. Although not shown, the exposure section 10 includes conventional optics for directing the image light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The sensor 12, which includes a two-dimensional array of photosites providing a predetermined picture resolution corresponding to the number of picture elements of the image, is a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. Preferably, the sensor 12 is a high resolution device such as the model KAF-1400 sensor, a 1320(H)×1035(V)-element full-frame CCD imager manufactured by the Eastman Kodak Company. The sensor 12 is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode 14, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter 16, which generates a digital image signal from the analog input signal for each picture element.

The digital signals are applied to an image buffer 18, which is a random access memory (RAM) with storage capacity for a plurality of still images. A control processor 20 generally controls the input section 2 of the camera by initiating and controlling exposure (by operation of the diaphragm and shutter (not shown) in the exposure section 10), by generating the horizontal and vertical clocks needed for driving the sensor 12, and for clocking image information therefrom, and by enabling the A/D converter 16 in conjunction with the image buffer 18 for each analog signal segment relating to a picture element. (The control Processor 20 would ordinarily include a microprocessor coupled with a system timing circuit.) Once a certain number of digital image signals have been accumulated in the image buffer 18, the stored signals are applied to a digital signal processor 22, which controls the compression and recording section of the camera. The processor 22 applies a compression algorithm to the digital image signals, and sends the compressed signals to a removable memory card 24 via a connector 26. A representative memory card is a 512 K-byte static random access memory (SRAM) available from Mitsubishi Corp. (A 1 megabyte memory card has been recently announced by ITT Canon.)

Since the compression and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer 28. (The processing buffer 28 may also be configured as part of the memory space of the image buffer 18.) The number of image signals needed in the image buffer 18 before digital processing can begin depends on the type of processing, that is, for a block transformation to begin, a block of signals including at least a portion of the image signals comprising a video frame must be available. Consequently, in most circumstances, the compression may commence as soon as the requisite block, e.g., of 16×16 picture elements, is present in the buffer 18.

The input section 2 operates at a rate commensurate with normal operation of the camera while compression, which consumes more time, can be relatively divorced from the input rate. The exposure section 10 exposes the sensor 12 to image light for a time period dependent upon exposure requirements, for example, a time period between 1/1,000 second and several seconds. The image charge is then swept from the photosites in the sensor 12, converted to a digital format, and written into the image buffer 18 during a standard rate, which may, for example, corresPond to a standard video field or frame rate. The repetition rate of the driving signals provided by the control processor 20 to the sensor 12, the A/D converter 16 and the buffer 18 are accordingly generated to achieve such a transfer. The processing throughput rate of the compression and recording section 4 is determined by the character of an image, i.e., the amount of detail versus redundant information, and the speed of the digital signal processor 22, and may take up to several seconds for an especially complex image. For this reason, the image buffer 18 shown in FIG. 1 provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. Further description of the operation of the image buffer is provided in the aforementioned, copending U.S. patent application Ser. No. 349,566.

In addition to the full resolution, compressed image, the digital signal processor 22 generates a reduced resolution, or "thumbnail", image from the original image and outputs the reduced resolution image, together with the compressed image to the memory card 24 as a multi-format image file. A multi-format image file with a "thumbnail" area as it would appear on the memory card 24 is shown in FIG. 2A for one image and in FIG. 2B for several images. In each case, the reduced resolution image signals occupy a defined area near the beginning of each image file. A header may be used before each image file (FIG. 2A) or a directory can identify the location of each image file (FIG. 2B) on the card. On request from the processor 20, the digital signal processor 22 recovers the "thumbnail" image from the image file and outputs it on a line 22a to a display device 30.

Inasmuch as the "thumbnail" image is itself low resolution, the display device 30 may be a low resolution electro-optical device such as a liquid-crystal display. Alternatively, the display device 30 can be of higher resolution and display the "thumbnail" image in a window or portion of the display space.

The "thumbnail" image may be generated by any one of several methods. Average values could be determined for given areas of the original image, or the original image could be subsampled over its entire area. The resulting "thumbnail" data could be grey-scale or full color, and the number of bits/per pixel could vary to suit the needs of the application. In any case, the criteria would be that 1) the "thumbnail" data should add a minimum amount to the overall file size and 2) the "thumbnail" image should contain enough information to present a recognizable representation of the original image.

The digital signal processor 22 compresses each still video image stored in the image buffer 18 according to the image compression algorithm shown in FIG. 1B. The compression algorithm begins with a discrete cosine transformation (block 33) of each successive block of the image data to generate a corresponding block of cosine transform coefficients. It is well-known that compression techniques are greatly enhanced when applied to image data which has been previously transformed in accordance with a discrete cosine transform algorithm. The "thumbnail" image data is preferably taken from the discrete cosine transformation (as will be explained) and applied to a file controller (block 40), which provides the "thumbnail" data on the line 22a to the display device 30 and combines the compressed data with the "thumbnail" data to provide the multi-format image file to the memory card 24.

The cosine transform coefficients are rearranged in serial order by a block-to-serial conversion step (block 34) described and illustrated in U.S. Pat. No. 4,772,956, "Dual Block Still Video Compander Processor," issued Sep. 20, 1988 to Roche et al, and which is assigned to the assignee of the present invention and incorporated by reference into the present patent application. The block-to-serial conversion step consists of arranging the discrete cosine transform coefficients in order of increasing spatial frequency, which corresponds to a zig-zag pattern illustrated in the Roche et al patent. The resulting serial string of transform coefficients is then subjected to conventional thresholding, normalization, and quantization (block 36) and minimum redundancy encoding (block 38). Thresholding discards data words of magnitudes less than a threshold number. Normalization entails dividing each data word by a divisor to yield a quotient. Quantization discards the fractional bits in the quotient. Minimum redundancy encoding is a technique well-known in the prior art for reducing the number of bits required to represent a frame of video information, without reduction in image quality, thereby greatly reducing the amount of storage that must be allocated to each still frame in the memory card 24.

The compressed video data does not emerge from the processor 22 as a standard-length stream of bits, but as a variable number of bits dependent upon the complexity of the picture and the rules used for truncating bits. The memory space, therefore, allocated for each image in the memory card 24 can vary from image to image. The processor 22, consequently, allocates memory space in the memory card 24 after each compression sequence for an image is completed so that the multi-format image files may be "packed" into the card as a continuum of compressed image data. This means the storage capacity, in terms of actual images, of the memory card is unknown in the beginning, and then gradually is specified as pictures are taken and the card is "filled". Alternatively, a fixed "maximum" space can be allocated in the memory card 24 for each multi-format image file; in this case, fewer images can be stored although the total capacity is always known.

What has been described to this point applies equally to monochrome or color pictures, except that color pictures require additional processing. For instance, if a multi-spectral color filter array (shown in broken line 39 in FIG. 1A) overlies the image sensor 12, the various colors are sorted out and processed differently for each color. This would be accomplished by an additional routine in the digital signal processor 22. Such color filter array processing would precede the discrete cosine transform block 33 (FIG. 1B) so that image compression can be done separately on each color and three compressed frames would be stored in the memory card 24 for each image.

Despite the degree of compression, a high quality digital image derived from a high resolution sensor can be large and, due to the necessity of decompression or expansion, require significant amounts of time to display due to size, resolution, and compression schemes. In keeping with the invention, the "thumbnail" or reduced resolution image is added to the compressed digital file format to make reviewing the image at any point in the imaging chain very fast. In terms of the multi-format file, a "thumbnail" image is a much smaller data file added to the original image data file. Although the image file may vary in length due to compression techniques, the "thumbnail" image would always be a known size based on the number of pixels in the original image.

An example would be a 1,280 by 1,024 pixel, 24-bit per pixel, compressed original image stored on a RAM-card mass storage device. This file might take on the order of 100 to 300 kilobytes of storage area depending on compression type. To display the image, it must first be expanded, and the resulting 4 Megabytes of information transferred to a display device. A "thumbnail" image is constructed by using the average value of each 16 by 16 pixel area in the original image to represent each pixel of the "thumbnail" image. If each pixel has an 8-bit grey scale, this would add about 5 Kilobytes to the overall image file size. To display the "thumbnail" image, no expansion is necessary, and only 5 Kilobytes of information needs to be transferred to the display device. The resulting image would be of sufficient quality to identify the subject matter of the original.

A "thumbnail" image generated from average values is preferable to one generated by simple subsampling (throwing away all but one pixel in a block). The averaged image looks more like the original with much less "blockiness" and less loss of detail. The preferred method for generating the "thumbnail" images uses the average or dc values from the DCT (Discrete Cosine Transform) algorithm, which were generated for compression of the image. The DCT algorithm produces one dc value for each block of the image being compressed. The dc value is a set of red, green, and blue values which are the mathematical average of the red, green and blue planes of pixels in the block. Alternatively, the mathematical average can be calculated outright over a block of pixels. This is done by actually

summing all the red values and dividing by the number of pixels to create an average red value, and then repeating for the green and blue planes.

A simplified block diagram is shown in FIG. 3A of a still video player for reproducing a picture or for making a hard copy print from the digital image signals stored in compressed format in the memory card 24. With the card 24 inserted into a connector 100, the digital signals are accessed and processed in the decoder 102. The stored dc component of the transform (the "thumbnail" data) is directly applied to a selector 104 while the compressed image data is applied to an expander 106. An expansion algorithm, which is the conventional inverse of the compression algorithm of FIG. 1B, is shown in FIG. 3B and implemented by the expander 106 which includes a conventional sequence of minimum redundancy decoding (block 106a), denormalization (block 106b), serial-to-block conversion (block 106c), and inverse discrete cosine transformation (block 106d). The digital image data is expanded block-by-block and stored in an image buffer 108 as a decompressed image. A conventional thermal printer 110 is connected to the buffer 108 for making a hard copy thermal print from the decompressed image. The output of the image buffer 108 is also connected to the selector 104, which is under control of an operator-designated selection routine 112. When a "thumbnail" image is to be observed, the selector 104 routes the "thumbnail" data through a digital-to-analog (D/A) converter 114 to a conventional CRT monitor 116. Alternatively, the decompressed image signals are converted to analog form by the digital-to-analog (D/A) converter 114 and displayed on the conventional CRT monitor 116.

A principal advantage of the file format shown in FIGS. 2A and 2B is that an image, with its associated "thumbnail" representation, can be easily separated from the collection of images on the memory card 24 and transmitted to external devices for further processing. For instance, the image file can be sent to the printer 110 and the "thumbnail" image can be quickly examined on the monitor 116 before committing to a print. Likewise, an image file can be easily downloaded to a transceiving device (not shown) and the "thumbnail" image can be examined before deciding to transmit. If the entire image file is transmitted, the "thumbnail" image can be quickly recovered at the receiving end for a preview of the final image. Moreover, for a plural number of images, the corresponding "thumbnail" images can be quickly accessed and displayed either in a mosaic frame or in sequence in order to select the desired full resolution image for printing, displaying, transmitting, etc. Furthermore, the "thumbnail" images can be played back by a dedicated player such as illustrated in FIG. 3A or by a personal computer or like device that is programmed to accomplish the functions outlined in FIG. 3A. In the latter case, the personal computer forms the interface between the memory card 24 and a printer, a monitor, a transceiver, etc.

The invention has been described in detail with particular reference to a presently preferred embodiment, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

What is claimed is:

1. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites corresponding to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

- means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;
- means for subsampling said digital image signals to generate reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;
- means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said digital image signals and are commonly accessible therewith for display and processing; and
- means for storing the image file in said digital memory.

2. The apparatus as claimed in claim 1 further including:

- display means for generating a display image;
- means for selecting an image file stored in said digital memory; and
- means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

3. The apparatus as claimed in claim 1 in which the sensor is sequentially exposed to a plurality of still images, said digital image signals and said reduced resolution image signals therefore corresponding to said plurality of images, said file generating means generating a separate multi-format image file for each still image from the digital image signals and the reduced resolution signals corresponding thereto, and said storing means storing each multi-format image file in said digital memory.

4. Electronic still imaging apparatus employing digital processing of image signals acquired from a plurality of still images and storage of the processed image signals in a removable digital memory, said imaging apparatus including an area image sensor having a two-dimensional array of photosites corresponding to picture elements of an image and means for exposing said sensor to image light so that analog image information is generated in respective photosites for each acquired image, said imaging apparatus comprising:

- means for converting the analog image information into digital image signals corresponding to respective picture elements;
- an image buffer for storing digital image signals corresponding to blocks of picture elements;
- digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed signals;
- means responsive to said stored digital image signals for generating reduced resolution image signals corresponding to a reduced resolution version of each image;
- means for forming a multi-format image file representative of plural versions of each acquired image,

each image file including the reduced resolution image signals and the compressed signals for a particular still image; and

means for downloading said image file for each acquired image to said removable digital memory.

5. The apparatus as claimed in claim 4 in which the reduced resolution image signals are generated from an average value of the digital image signals corresponding to each block of picture elements.

6. The apparatus as claimed in claim 5 in which the average values of the digital image signals are derived from the transform coefficient signals.

7. Electronic image processing apparatus employing digital processing of image signals corresponding to picture elements of a still image and storage of the processed image signals in a digital memory, said image processing apparatus comprising:

an image buffer for storing digital image signals corresponding to blocks of picture elements;

digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed image signals, said digital processing means further generating reduced resolution image signals from said stored digital image signals;

means for generating a multi-format image file representative of plural resolutions of the still image, said image file including the reduced resolution image signals and the compressed image signals; and

means responsive to said digital processing means for downloading the image file to said digital memory.

8. Apparatus as claimed in claim 7 in which said digital processing means generates an average signal for each block of stored digital image signals and said reduced resolution image signals are formed from said average signals.

9. An electronic image processing system employing digital processing of image signals corresponding to picture elements of a still image and storage of the processed image signals in a digital memory, said image processing system comprising:

an image buffer for storing digital image signals corresponding to blocks of picture elements;

digital processing means for transforming blocks of stored digital image signals into corresponding sets of transform coefficient signals and for encoding the transform coefficient signals into a stream of compressed image signals, said digital processing means further generating reduced resolution image signals from said stored digital image signals;

means for generating a multi-format image file representative of plural resolutions of the still image, said image file including the reduced resolution image signals and the compressed image signals;

means responsive to said digital processing means for downloading the image file to said digital memory;

means for selecting an image file stored in said digital memory; and

playback means for operating on the selected image file and generating a reduced resolution image display from said reduced resolution image signals.

10. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites correspond-

ing to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;

means for averaging said digital image signals over local areas of the still image to generate reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;

means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said digital image signals and are commonly accessible therewith for display and processing; and

means for storing the image file in said digital memory.

11. The apparatus as claimed in claim 10 further including:

display means for generating a display image;

means for selecting an image file stored in said digital memory; and

means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

12. Electronic still imaging apparatus employing digital processing of image signals corresponding to a still image and storage of the processed image signals in a digital memory, said imaging apparatus including an image sensor having an array of photosites corresponding to picture elements of the still image and means for exposing said sensor to image light so that analog image information is generated in respective photosites, said imaging apparatus comprising:

means for converting the analog image information into digital image signals corresponding to a predetermined picture resolution;

means operating on blocks of digital image signals for compressing said digital image signals and generating averages over said blocks;

means responsive to said averages produced by said compressing means for generating reduced resolution image signals corresponding to a picture resolution lower than said predetermined resolution;

means for generating a multi-format image file representative of plural resolutions of the still image from the combination of said compressed digital image signals and said reduced resolution image signals, said combination forming a singular file structure in which said reduced resolution image signals occupy a defined file area in relation to said compressed digital image signals and are commonly accessible therewith for display and processing; and

means for storing the image file in said digital memory.

13. The apparatus as claimed in claim 12 in which said compressing means compresses the digital image signals in a plurality of stages, one stage including the performance of a discrete cosine transform on blocks of digital

image signals and another stage including minimum redundancy encoding of the transformed image signals.

14. The apparatus as claimed in claim 13 wherein said discrete cosine transform produces a dc component and said reduced resolution image signals are generated from the dc component of the discrete cosine transform.

15. The apparatus as claimed in claim 12 further including:

display means for generating a display image;

means for selecting an image file stored in said digital memory; and

means for applying said reduced resolution image signals from said stored image file to said display means to generate a low resolution display of the still image.

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EXHIBIT NO. 4

EXHIBIT NO. 4

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